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Implementation of Discrete Wavelet Transform Processor For Image Compression

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Abstract

Image compression is one of the major image processing techniques . Discrete wavelet transforms is the most popular transformation technique adopted for image compression. This paper presents an efficient VLSI architecture of a high speed, low power Discrete Wavelet Transform computing. There are number of architectures present for realizing DWT. Based on the application and the constraints imposed, the appropriate architecture can be chosen. Proposed DWT architecture uses DA-DWT scheme that is suitable on FPGA. The architecture has regular structure,simple control flow,small embedded buffers and low power consumption.

Keywords: *Discrete Wavelet Transforms (DWT), Distributive Arithmetic (DA), JPEG2000, VLSI architecture, FPGA implementation.*

1. Introduction

Image compression, is the science of reducing the amount of data required to represent an image. It is one of the most useful and commercially successful technologies in the field of digital image processing. Digital image and video compression is now very essential. Internet teleconferencing, High Definition Television (HDTV), satellite communications and digital storage of movies would not be feasible unless a high degree of compression is achieved.

As images convey more information to a user, it is many of the equipment today have image displays and interfaces Today's electronic equipment comes with user friendly interfaces such as keypads and graphical displays.. Image storage on these smaller, handled devices is a challenge as they occupy huge storage space; also image transmission requires higher bandwidth. Hence most of the signal processing technologies today has dedicated hardwares that act as co-processors to compress and decompress images. With the increasing use of multimedia technologies, image compression requires higher performance. To address needs and requirements of multimedia and internet applications, many efficient image compression techniques, with considerably different features, have been developed.

As the technology of semiconductor industries has enormous growth it has led to unpredictable demand for low power, high speed complex and reliable integrated circuits. These circuits are used for medical, defence and consumer applications. Today's electronic equipment comes with user friendly interfaces such as keypads and graphical displays. As images convey more information to a user, it is many of the equipment today have image displays and interfaces. Storage of image requires higher bandwidth image storage on these smaller, handled devices is a is a very difficult task as they occupy huge storage space, also image transmission requires higher bandwidth. Hence most of the signal processing technologies today has dedicated hardwares that act as co-procesors to compress and decompress images.

To fulfill such kinds of needs and requirements of multimedia and internet applications, many efficient image compression techniques, with considerably different features, have been developed. Over the past several years, the wavelet transform has gained widespread acceptance in signal processing and in image compression research in particular. Traditionally, image compression adopts discrete cosine transform (DCT) in most situations. DCT has been applied successfully in the standard of JPEG, MPEGZ, etc. However, the compression method that adopts DCT has several shortcomings that become increasing apparent.

Traditionally, Fourier transforms have been utilized for signal analysis & reconstruction. However, Fourier transform does not include any local information about the original signal.Therefore, Short Time Fourier Transform (STFT or Gabor transform) has been introduced, which uniformly samples the time-frequency plane. Unlike the STFT which has a constant resolution at d times and frequencies, the wavelet transform has a good time and poor frequency resolution at high frequencies, and good frequency and poor time resolution at low frequencies . In JPEG2000, Discrete Wavelet Transform is used as a core technology to compress still images. The DWT has been introduced as a highly efficient and flexible method for sub band decomposition of signals [13]. The two dimensional DWT (2D-DWT) is nowadays established as a key operation in image processing.It is multi-resolution analysis and it decomposes images into wavelet coefficients and scaling function., In Discrete Wavelet Transform, signal energy concentrates to specific wavelet coefficients. This characteristic is useful for compressing images.. In addition to image compression, the DWT has important applications in many areas, such as computer graphics, numerical analysis, radar target distinguishing and so forth. For this purpose, a cutting window is used. This window is known as “Mother Wavelet”. The problem here is that cutting the signal corresponds to a convolution between the signal and the cutting window. The signal will convolve with the specified filter coefficients and gives the required frequency information. The decomposition of the image using 2-level DWT is shown in figure-1 .

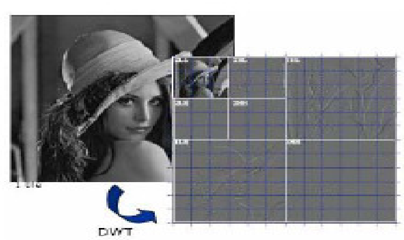

Fig1. Decomposition of Image

2.Discrete Wavelet Transform

Wavelets convert the image into a series of wavelets that can be stored more efficiently than pixel blocks. Although wavelets also have rough edges, they are able to render pictures better by eliminating the “blockiness” that is a common feature of DCT based compression [7]. Not only does this make for smoother color toning and clearer edges where there are sharp changes of color, it also gives smaller file sizes than a JPEG image with the same level of compression

2.1 One-Dimensional Discrete Wavelet Transform

Two main methods exist for the implementation of 1D-DWT: the traditional convolution-based implementation[14] and the lifting-based implementation [5].

2.2 Two-Dimensional Discrete Wavelet Transform

The basic idea of 2-D architecture is similar to 1-D architecture. A 2-D DWT can be seen as a 1-D wavelet scheme which transform along the rows and then a 1-D wavelet transform along the columns,.The 2-D DWT operates in a straightforward manner by inserting array transposition between the two 1-D DWT. The rows of the array are processed first with only one level of decomposition. This essentially divides the array into two vertical halves, with the first half storing the average coefficients, while the second vertical half stores the detail coefficients. This process is repeated again with the columns, resulting in four sub-bands (see Fig. 2) within the array defined by filter output. Fig. 2 shows a three-level 2-D DWT decomposition of the Lena image.

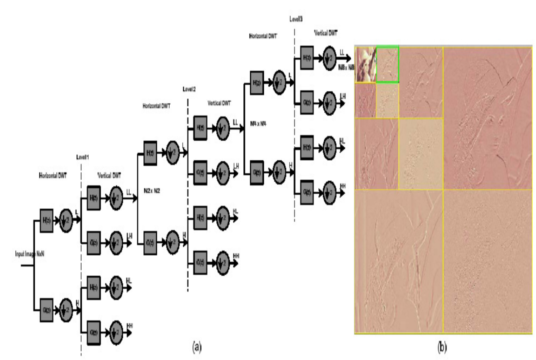

Fig 2. Three level decomposition for 2D – DWT

Image consists of pixels that are arranged in two dimensional matrix, each pixel represents the digital equivalent of image intensity. In spatial domain adjacent pixel values are highly correlated and hence redundant.. In order to compress images, these redundancies existing among pixels needs to be eliminated. DWT processor transforms the spatial domain pixels into frequency domain information that are represented in multiple sub-bands, representing different time scale and frequency points.

One of the prominent features of JPEG2000 standard, providing it the resolution scalability [3], is the use of the two-dimensional Discrete Wavelet Transform (2D-DWT) to convert the image samples into a more compressible form. It is considered as the key difference between JPEG and JPEG2000 standards. Since there is no need to divide the input image into non-overlapping 2-D blocks and its basis functions have variable length, wavelet-coding schemes at higher compression ratios avoid blocking artifacts. Hence the compression artifacts are dispersed over a correspondingly larger area, and reducing the visual impact.

Let Human visual system is very much sensitive to low frequency and hence, the decompose data available in the lower sub-band region and is selected and transmitted, information in the higher sub-bands regions are rejected depending upon required information content. Up to now, much work has been performed on DWT theory and many VLSI architectures have been proposed. paper [1] summarizes various schemes. Most popular one is the DA-DWT scheme that is suitable on FPGA, as it consumes fewer resources and has high throughput.

3.DWT Architecture

In this work, a modified DA-DWT architecture is designed based on the work reported in [15].This architecture uses Haar Transformation technique.The hardware architecture is shown in Fig. 4. It calculates the 2D-DWT in row-column fashion on the input image. The row filter calculates the DWT of each row of the external memory image data.Then, the resulting decomposed high-pass and low-pass coefficients are stored in intermediate buffers, and the column filter calculates the vertical DWT as soon as there are sufficient coefficients generated by the row filter. The architecture framework is composed of the following parts: two 1D-DWT blocks, internal buffers, LL FIFO used for multilevel decomposition, Address generator block and Controller block.

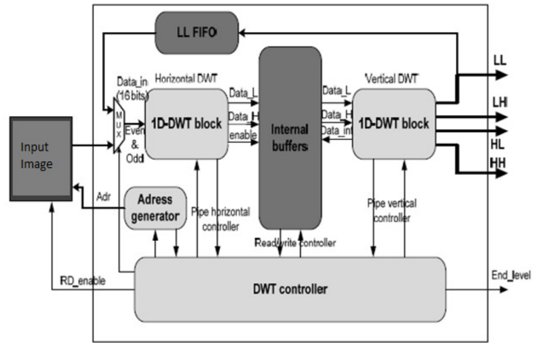

Fig 3.The block diagram of DWT architecture

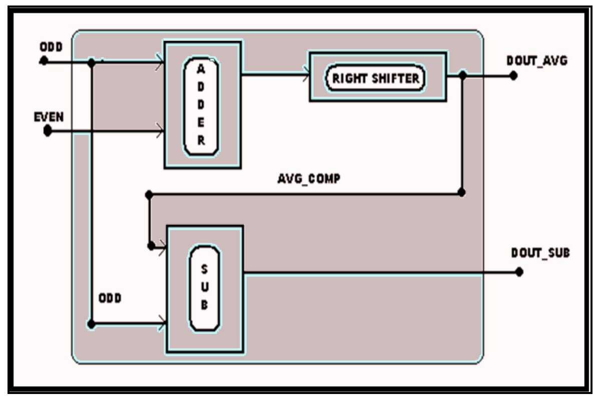

Fig 4. Block diagram of DWT System

The fig 4. Shows DWT System in which adder,substractor and right shifter are used to find out avg and difference components first even and odd samples are given to the adder then output of adder right shifted by one to give average components . The difference component is calculated by substracting average and odd components. HDL model for the architecture uses Verilog it is simulated by using Xilinx.

4.Simulation Results for Dwt System

These are the simulation results for DWT system in which we have given input image text file and we got corresponding average and difference components values and their corresponding addresses are shown in simulation results.

After simulation in order to see compressed image MATLAB is used.

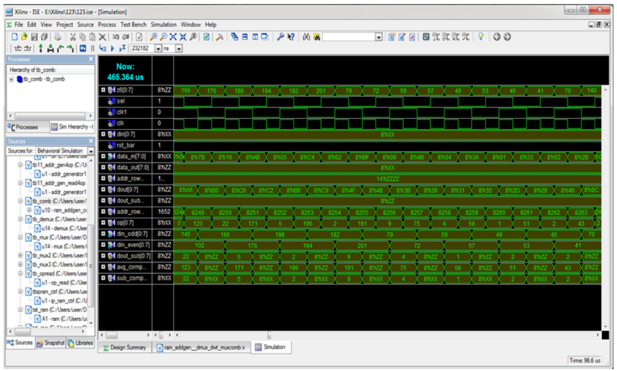

Fig 5. Simulation result of DWT system

After simulating the verilog integrated module in order to extract image we have taken help of MATLAB.\

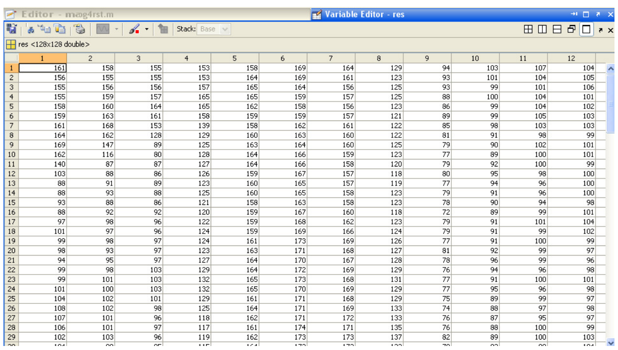

Fig 6. Verilog program output using MATLAB

Fig 7. Compressed Image

Fig 7 shows the final compressed image by using Verilog. In order to compare these results we will do comparision by using MATLAB.

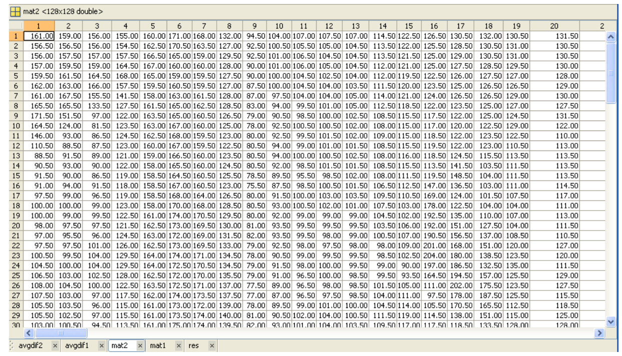

Fig 8. Results using MATLAB

From the results shown in fig 6 and fig 8 we got approximately same results. From this results we can say that proper compression has been achieved by using proposed architecture.

5.Conclusion

In this paper, we have proposed a VLSI architecture to meet the requirements of real-time image and video processing. It can provide fast computing time, low power consumption. This hardware is proposed to design to be used as part of a complete high performance and low power JPEG2000 encoder system.

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