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Design and Implementation of Four Level Asynchronous Counter Using D-Flipflop

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Abstract - A quaternary asynchronous counter is proposed using D-flip-flop, here D-flip is used as a basic building block for the design of counter a mod-16 asynchronous counter using D-flip-flop is presented in this paper. Quaternary multiplexer and Flip-flop are used to design quaternary asynchronous counter. In this paper binary D-flip-flop compared with quaternary D-Flip-flop and simulation of quaternary circuit done using H-spice software. Performance evolution of Proposed D-flip-flop is compare with existing flip-flop with optimization of power and delay. The proposed asynchronous counter has less power dissipation and propagation delay.

Keywords – *Multiple Value Logic (MVL), Quaternary Logic, MVL Counters,. Sequential Circuit.*

1. Introduction

Multiple value logic has lot of applications like reduction in chip area it is useful for high speed image processing Nowadays people are working on computational technique of binary number system .Computational system are designed using binary logic only.
People are now interested to working on multiple value logic for fast computing technique. They Decimal number system is a alternative for binary number system as they could produced reliably and inexpensively.
The present state of technology is more favorable to implement lower radix systems.
In real life situations, there is no clear cut binary yes/no requirement; situations such as yes/no not defined, or up/down/stop, or left/right/straight ahead bound in the real world scenario. In binary there are only two situations yes /no but situation such as yes/no not defined or up/ down//stop or left/right/straight ahead exist in real world scenario Due to this 3-valued logic or ternary logic is more appreciable than binary and digital realization is more appropriate than binary [6] Higher radix reduces number of interconnection per system or subsystem. Due to higher radix information carrying capacity of each connection increases [7] In this paper we are preparing sequential circuit using multiple value logic or quaternary logic. For describing quaternary logic first we describing primary logic levels o and 1 and Boolean logic.[2] Shannon's proved that a two valued Boolean algebra can describe operation of two valued switching circuit Now a days Boolean algebra and Boolean functions are required in computer chips and integrated circuit.

As the radix of system increases, the difficulties in the minimization or reduction of logic function is get increases. It becomes difficult to for higher radix to reduce the function design equation. There are three directions for the work in MVL. Due to pressure to reduce interconnection complexity and reduce chip area on VLSI, it is giving motivation for the investigation of many different hardware implementations of MVL systems. The largest commercial use of Multiple-Valued logic is in the area of MVL memories. The MVL can be used to overcome existing difficulties in the analysis of problems in binary digital systems, such as the design of fault simulators. Finally there is still ongoing work in the general area of switching theory to yield the best.

Scientist Venn's represented binary logic level using diagram in 1984 fig1 (a) represent two variable example.

Fig 1 represent a three variable example which consist of 256 linear Boolean function [9]

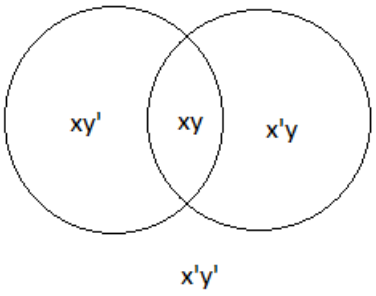

Figure 1: Venn diagrams representing for a two variable map, *n* =.2

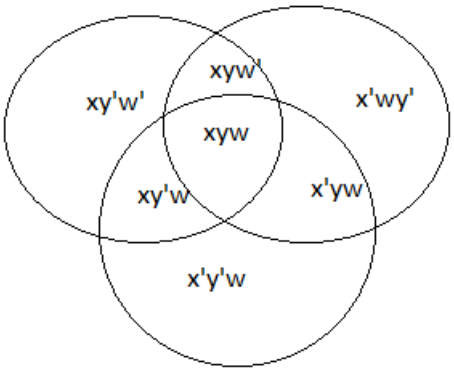

Figure 2: Venn diagrams representing for a two variable map, n=3

Boolean algebra is a model of Boolean logic, any algebraic system is model of classical logic that works on truth value values TRUTH and FALSE However in a real life situations observation do not comply with TRUE and FALSE values and there is always uncertainty in deciding these values.

One has to accept multiple decisions like to what extend decision may be true and to what extend the decision may be false [8]

2. Multi-valued Logic

Binary number system used for traditional calculations and Multiple value logic consist of more than two values. Multiple value logic system has lot of advantage over binary. Expanding existing levels to ternary and penta levels, higher processing rate is achieved in various applications like memory management and communication

Binary logic technology has come across the dramatic changes and advances. Earlier from electro-mechanical to electronic switches by using electronic tubes (1919) like triode, pentodes, then from tubes to transistors (1948) and from transistors to LSI (1958) and VLSI (1970)circuits. Although efficient and powerful, binary logic is not the most efficient and powerful switching logic. Non-binary logic or Multiple Valued Logic (radix>2) has been around for quite a while and is known as Multi-Valued Logic or Many Valued Logic. In this paper it will be referred to as MVL hereafter. The subject of MVL is also known as Multi-Valued, Multiple-Valued or Many-Valued logic. In case of 3-Valued logic (radix = 3) the term 'Ternary' logic is used & term 'Quaternary' logic (radix = 4) for 4-Valued logic and so on up to 'n' values. Multi-Value logic is regarded as a switch with more than two states. Such as a three- value switch with logic states '0', '1' and '2', 4-value switch with logic states '0', '1', '2' and '3' and so on up to 'n' values.

MVL has been the topic of most interest of many researchers over the last 50 years. From 1971 there has been an annual symposium devoted exclusively to the object.

Moreover, a large number of technical papers have published together with numerous survey articles. Much of the ancient work is purely theoretical nature concerned with the completeness of the function with sets of operator, function minimization and similar problems from the switching theory and logic design. Work on hardware implementation of multiple value devices has been more recent. The use of Multi-Valued logic ranges from various applications to VLSI technology and design techniques. An advantage of a ternary representation over binary is economy of digits to represent. A number in binary system one need 58% more digits than ternary [7] For example, to represent a 15-digit decimal number, one requires 34 ternary digits instead of 54 binary digits. Ternary representation admits sign convention also.. The most significant advantage is that there is reduction in the interconnection required to implement a logic function. This in turn causes reduction in the chip area while fabricating devices [8]. Addition to the design it is also necessary to assess the cost of manufacturing of these types of multiple valued logic circuits

$$C = k(R*D) = k\left[R\,\frac{\text{Log } N}{\text{Log } R}\right] \qquad \text{----------(1)}$$

Let R be the radix, 'D' be the number of digits to express a range of N numbers such that N = RD. Assume that the number and/or cost of the basic hardware components C is proportional to the "digit capacity" R x D, then we have Where k is some constant. Differentiating this cost equation with respect to the radix R and equating to zero gives that R should equal e (2.718) for minimum cost. From this analysis R=3 should be more economical than the binary radix R=2. If we consider that devices or circuits are available which provide two, three, four or more stable digital signals without any increase in individual costs for the higher-valued radices, then in such ideal circumstances total cost C would be proportional to D. Hence,

$$C = k(R*D) = k\left[R\,\frac{\text{Log } N}{\text{Log } R}\right] \qquad \text{----------(2)}$$

which is a gradually decreasing total cost C with Increasing R [10, 11, and 12].

Table 1 shows representation of decimal numbers using Ternary symbols. The decimal number D in terms of Ternary symbol is given in equation 3

D = {Tn3n+Tn-13n-1+…+(T1 3 1)T030} ----------(3)

Where T = ternary digit -1, 0, +1

Tn = most significant
n = significance of the ternary digit,

However, the -1, 0, +1 numbering system has a unique advantage that any number can be changed from a positive value to the corresponding negative value by merely changing all -1s to +1s and vice versa, leaving all zeros unchanged [12]. Here Table-2 shows natural representation of quaternary numbers.

Table 1: Representation of decimal numbers using ternary symbols.

Decimal number D	**Ternary notation using the number -1,0,1**
0	0000
1	0001
2	000-1
3	0010
4	0011
5	01-1-1
6	01-10

Table 2: Natural representations of quaternary numbers

Quaternary logic representation	**Natural Representation**
0	00
1	01
2	10
3	11

Organization of the paper is as follows: Discussion regarding previous work is illustrated in section 3. Sequential circuit design is done in section 4. In the same section quaternary D flip-flop and quaternary counters are explained. Results are discussed in section 5. Finally conclusion is given in section 6.

3. Sequential Circuit Design

3.1 Quaternary D-flip flop

D-flip-flop is called as data flip-flop here, a quaternary D-flip-flop has four stable states, namely 0, 1, 2 and 3 A quaternary positive edge triggered D-flip-flop is designed with a synchronous input 'Din' and two synchronous in asynchronous inputs clear and preset.

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Synchronous or asynchronous term is with reference to clock. Input 'Din' is being synchronous can change the output only at positive edge of clock. It means when a low (0V) to high (3V) transition occurs. Since preset and clear are asynchronous, any change in them affects the output immediately, irrespective of positive edge of clock. Preset and clear are both active low inputs. Hence logic 0 on preset input line causes the output to enter into logic 3 states and logic 0 on clear input line causes the output to enter into logic 0 state.

If both preset and clear are active low simultaneously then the Output is unpredictable. Hence this condition must be avoided. The truth table and circuit diagram for D-flip flop are as shown in table 3 and figure 5 respectively..

The block diagram for D-flip flop is shown in figure 3. If preset and clear are both logic 3 then din appears at the output at positive edge. If preset = 0 and clear = 3 then output = 3. At this stage flip flop is in set state. If preset = 3 and clear = 0 then the output = 0. Now the flip flop is in clear or reset state.

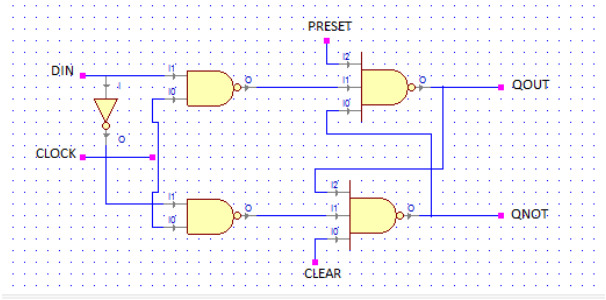

Figure 3: Circuit Diagram of Quaternary D-flip flop

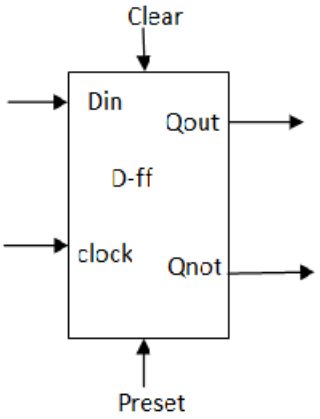

Figure 4: Block Diagram of Quaternary D-flip flop

Table 3: D-flip flop truth table for quaternary logic .

Inputs				Outputs	
Preset	Clear	Din	Clock	Q+	Qbar+
0	3	X	X	3	
3	0	X	X	0	
0	0	X	X	UNPREDICTABLE	
3	3	0	↑	0	3
3	3	1	↑	1	2
3	3	2	↑	2	1
3	3	3	↑	3	0

4. Two Digit Asynchronous Quaternary Up Counter Using Quaternary Multiplexer

The control unit 1 for producing the least significant digit and control unit 2 producing most significant digit of the counter output is as shown in figures 7 and 8 respectively. They make use of quaternary multiplexers [24] and D-flip flops. The D-flip flop designed above has been used.

This asynchronous counter has sixteen states as shown in table 4.Here Q1 is the most significant digit and Q0 is the least significant digit. The outputs of the flip flops are fed back to the multiplexers [24] to get the next count (next state). Initially the D-flip flops are reset using the clear input to Get the initial count (initial state) 00. Once reset, the next count sequences are obtained one after the other at subsequent positive clock edges provided clear and preset are inactive. Counts occur only at positive edge of the clock since the flip flops are positive edge triggered. It must be noted that the counter can be brought to reset state at any instant using the clear input.

Control unit I: Generation of least significant bit of asynchronous counter

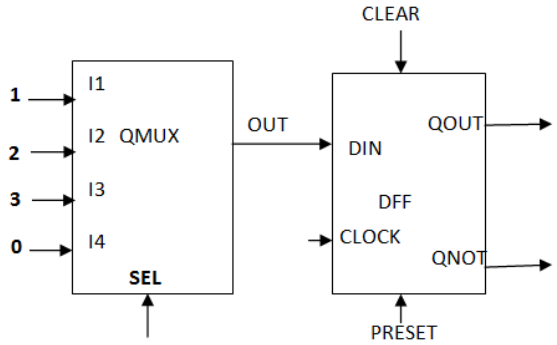

Figure 5: Circuit for generating least significant digit of counter output.

CONTROL UNIT2: Generation of most significant bit of asynchronous counter

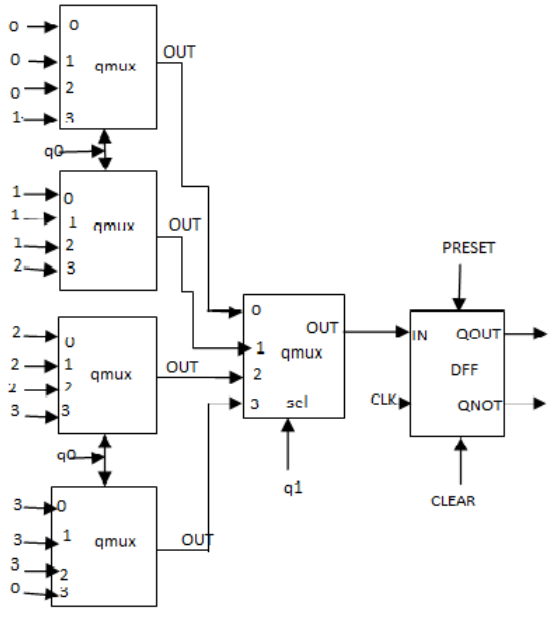

Figure:6 Generation of most significant bit of counter output

Table4 :.State table of Quaternary Up-counter

Present state		Next state	
Q1	Q0	Q1+	Q0+
0	0	0	1
0	1	0	2
0	2	0	3
0	3	1	0
1	0	1	1
1	1	1	2
1	2	1	3
1	3	2	0
2	0	2	1
2	1	2	2
2	2	2	3
2	3	3	0
3	0	3	1
3	1	3	2
3	2	3	3
3	3	0	0

5. Results and Discussion

The simulation results for the quaternary D-flip flop and the quaternary up-counter are shown in figure 9 and 10 respectively. Simulation is carried out using Synopsys Hspice Tool and results are observed as follows.

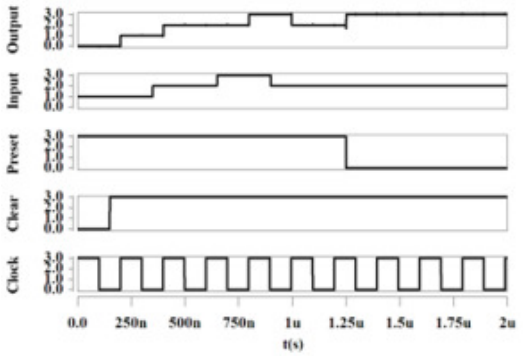

Figure 7: Simulation result of quaternary D-flip flop

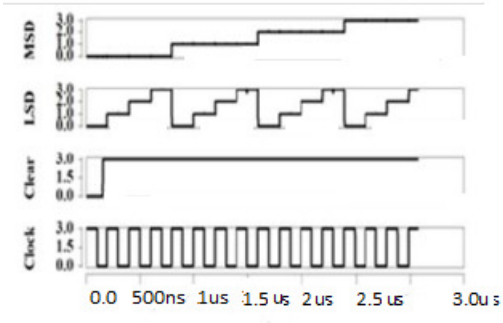

Figure 8: Simulation result of quaternary counter

Table 5: Performance parameters comparison of different D-flip flops

Flip flop	author	foun dry	Max supply voltage	Dynamic power dissipatio n µwatt	Delay ns
Binary Flip flop	Sung [26]	0.18 µm	1.5v	47.8	0.224
	Shin[27]	0.35 µm	3.3v	540	0.427
	Do[25]	0.18 µm	1.8v	4.7	0.138
	Elgamel[24]	0.18 µm	3.3v	19.84	0.224
Multi-valued flip flop	Q-IDEN[19] DFF	350 nm	3.5v	138	0.43
	NMIN [18]TG DFF	350 nm	3.5v	880	29
	Proposed dff	**180 nm**	**3.0v**	**56.19**	**1.187**

The average power dissipation and propagation delay of the quaternary D-flip flop are compared with Q-IDEN D flip flop [19] [21].The comparison results are as shown in table 6. The average power dissipation and propagation delay of the counter is shown in table 7

. Table 6.Power and delay of counter

Average power dissipation in µwatt	23.705
Propagation delay in ns	1.0163

2D-Flip-flop shown in this paper has both preset and clear input. By using these input asynchronous counter is implemented. This D-flip flop has less average power

dissipation (56.19 μW) the propagation delay (1.187ns) is found to be slightly higher compared to Q-IDEN D flip flop. The increase in propagation delay can be neglected when compared to its functional advantages. It must be noted that the Q-IDEN D-flip flop has no preset and clear input and hence cannot be used for designing counters. The counter designed using Quaternary D-flip flop has a propagation delay of 1.1963 ns and average power dissipation of 24.805 Mw.

6. Conclusion

Flip-flop used here are storage devise in designing of multiple value sequential circuit. . In this paper, quaternary D flip-flop with preset and clear is designed this quaternary D flip-flop is compared to previously designed binary and multi-valued D flip-flops. Proposed D flip-flop is better than all other flip-flops reported so far except propagation delay. Propagation delay is slightly higher in our flip-flop. But power dissipation is 64.33% less than at of DLC based D flip-flop and Q-IDEN D flip-flop. 2 bit ary counter can count only up to 4 counts, where as 2 bit quaternary counter can count up to 16. Multiple valued counters are simple dividers that are basic components in most digital systems and can generate a multiple-valued output. 2 bit quaternary counter dissipates 24.705 μW of dynamic power. D flip-flop reported in this paper is useful for designing many low power sequential circuits such as counters, shift registers and state machines.

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