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Design of Digital Circuit for Low Power Communication Centric RF Transceiver in Wireless Sensor Node using VHDL

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Abstract- In wireless technology machines are talking with machines. The sensors have batteries as power backup. There is a serious issue of maintenance of these batteries and exchange of batteries, so there is a need of such a wireless sensor node which will consume very less power without affecting the functionality like speed, range and standard compliance. The power breakdown of wireless sensor node shows that the hungriest part is RF transceiver chip. So total power consumed by the sensor node can be reduced by reducing the power consumed by RF transceiver. The common solution is to activate the transceiver by changing the duty cycle. The duty cycle change is not correct solution because it has some drawbacks. So the possible solution to solve the issue is designing a digital control circuit which will activate the main radio after listening to channel and generating a interrupt as and when required. This on demand communication mechanism will reduce power wastage. The architecture of sensor node is to be modified to communication centric approach rather than traditional approach. The digital control circuit will wake up the transceiver as and when correct message will arrive at the input. The data packet is to be defined for the same. The digital circuit is using 2.4 GHz operating frequency. The power supply used is 1.8 V – 2.1 V. The circuit consists of analog front end comprising of LNA which amplifies the signal, a detector which detects the signal and decoder which retrieves the original signal from packet that arrives. Once the signal is decoded it goes to digital control block which is the main block of the circuit. The implementation is carried out in VHDL and program is run in Xilinx 14.7 software .A test bench is written in Verilog for simulation purpose. The simulation is carried in Isim software available in Xilinx 14.7 .The simulation of the code shows that the time required to write and read the data parameters is 16.4 uSec. Accordingly the performance analysis is carried out. First power consumption of CC2500 RF transceiver without digital control circuit is calculated. In active mode it comes out to be 20 uWatt. Then when the digital control circuit is present the power consumption of same RF transceiver is calculated, it comes out to be 0.034 pWatt. This shows that with the help of digital control circuit the power consumption is very less as compared to without digital circuit. The rest of the paper consists of System overview, experimental results, performance analysis and conclusion

Keywords*: RF, Wireless Sensor Node, Power Consumption, VHDL, Simulation*

1. Introduction

Wireless technology is nowadays very popular field. Machines are talking with machines. The wireless sensor and control use batteries as a power backup. The exchange and maintenance of batteries is serious issue. There is a need of such a wireless sensor node which will consume very less power. The power backup problem can be solved using energy harvesting [1] or energy scavenging. The main challenge to develop low power sensor network node is management of energy consumption without affecting the functionality like speed, range and standard compliance. Energy management deals with process of managing energy resources by means of controlling the battery discharge, adjusting the transmission power, and scheduling the power resources so as to increase the lifetime of the node. The energy efficiency of a sensor node is defined as amount of data delivered by node to the total energy expended. Higher the efficiency greater the number of packets delivered by node with given amount of energy reserve. To address the power consumption problem the common solution is to activate the transceiver periodically with the help of duty cycle. Due to variation in the application nature, communication latency and energy requirement the duty cycle requirement changes. The duty cycle strategy gives improvement in power consumption.[3] The node has to listen to communication channel for data (idle listening), or has to carry out over listening. Another drawback of duty cycle scheme is delay caused by receiver for receiving the data. The synchronization between transmitter and receiver is also technical challenge. So the possible solution to solve the issue is designing a digital circuit which will activate the main radio after listening to channel and generating a interrupt as and when required. This on demand communication mechanism will reduce power wastage. The traditional approach for low power radio sensor node architecture is processor centric. In this mode processor is main component which handles the transceiver. This requires additional power.

The same architecture can be modified to communication centric architecture as shown in figure below.

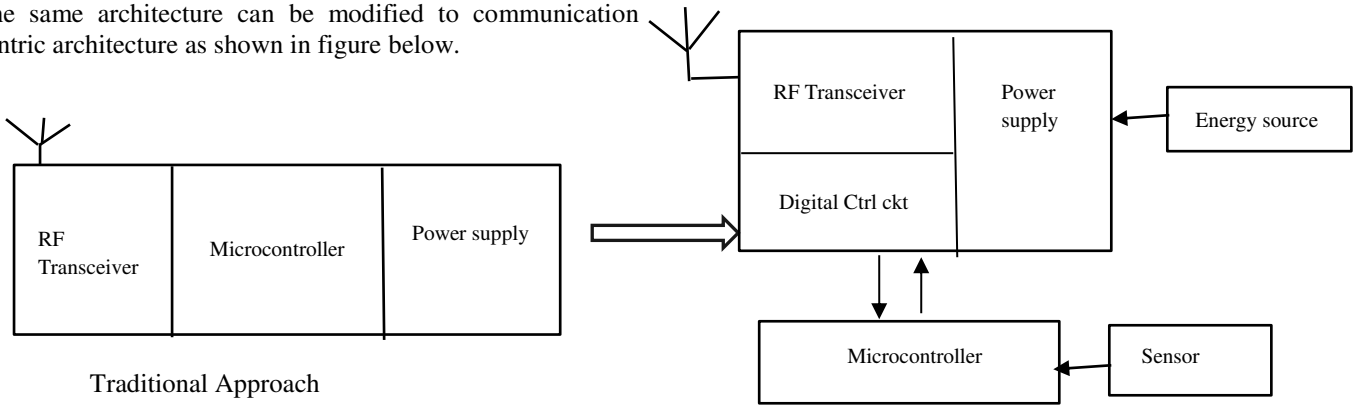

Fig 1: Traditional Approach Vs Communication centric approach

In this approach the transceiver acts independently and can transmit and receive data. This architecture reduces the power consumption significantly. The figure shows a digital control circuit which activates the RF transceiver and the Microcontroller [2] when correct message appears at the input channel. The power consumption for the two different architectures is shown in fig 2.

In order to avoid this, the nodes are switched off during idle conditions and switched on only when there is an arrival of request packet.[4] This provide two advantages: reducing the wastage in power consumed when the node is in listen mode, and providing idle time for the batteries of the node to recover charges.

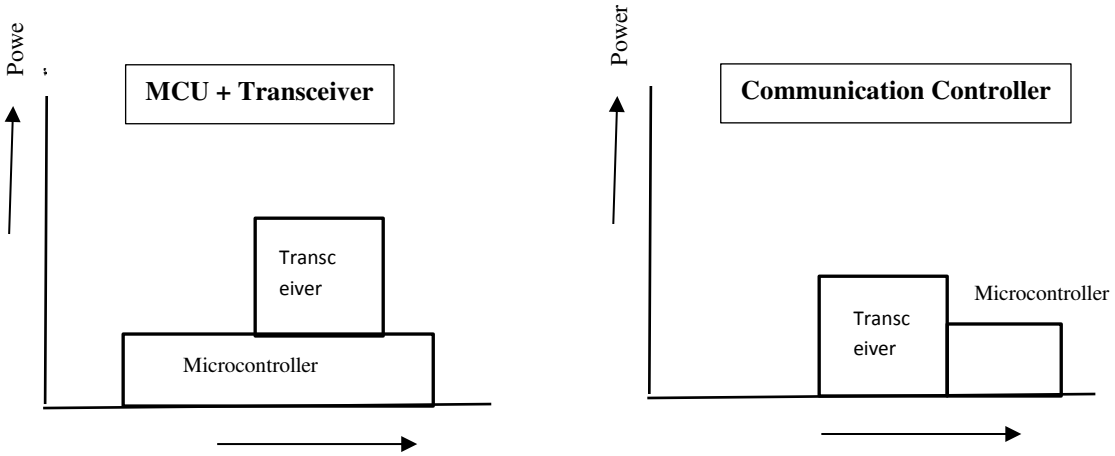

Fig 2: Power consumption for two different architectures

2. System Overview

Driven by the demand for "green" technology and better use of power, a new generation of extreme low power wireless networks is being developed for use in machine to machine network, for individual and control applications, as well as for health, security and other purposes. The nodes in the network consumes a substantial amount of power even when they are in an idle state since they are listening to the channel awaiting request packets from the neighbours.

Since the arrival of the packet is not known it is difficult to calculate the time duration for which the node has to be switched off. Most basic RF transceiver have their current consumption specified for three common modes of operation; namely standby mode, synthesize mode and full transmit and receive mode. The power profile of typical CC2500 RF transceiver is shown in fig 3 below. (Ref Ti.com). The power profile shows that major power consumption is in transmit and receive state. If we calculate the power consumption we can see that in active mode the power is 20 micro watt and in sleep mode it is 0.13 micro watt. This shows that if we keep RF transceiver in sleep mode for maximum time we can save a considerable amount of power.

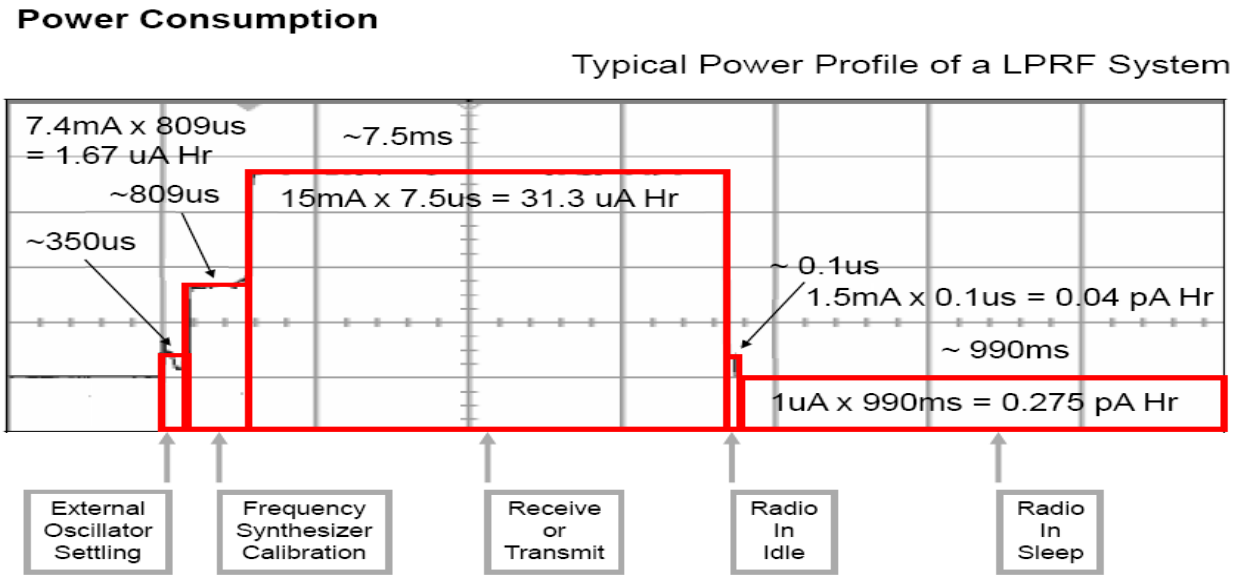

Fig 3: Power profile of CC2500 RF transceiver (Reference Ti.com)

This can be achieved by our digital control circuit. The main purpose of digital control circuit is to wake up the microcontroller and RF transceiver only when the correct data packet is arriving at the input. So a wake up data packet is to be defined. The format of the message depends upon the type of modulation used and the ease with which it is demodulated. Here OOK modulation is suitable since to demodulate the same some passive components are required [5]. The wake up message should contain start sequence (8 Bits) that initiate data packet, 8 bits for the node address, 26 bits for application Id, 12 bits for channel Id (4 bits for band and 8 bits for channel selection). The data packet will be as shown in fig 4 below consisting of 54 bits.

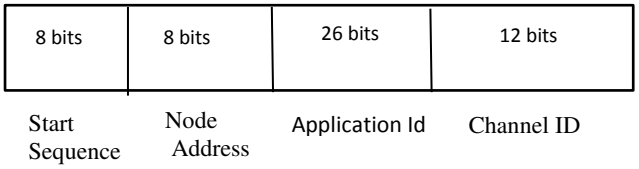

Fig 4: Wake Up message format

The error detection is to be taken into consideration. The Manchester encoding is useful out of the many encoding techniques. Manchester encoding is the coding technique that represents an original bit by another set of bits. For each bit of original data there are two bits for the Manchester encoding. Due to this the wake up message format becomes as shown in fig 5 below consisting of 100 bits. The start sequence is not encoded with Manchester encoding

The digital control circuit is using 2.4 GHz ISM band as operating frequency. The power supply used is 1.8 v to 2.1 V.

The circuit consists of analog front end comprising of LNA which amplifies the signal, a detector which detects the signal and a decoder which retrieves the original signal from the packet arrived (Data Signal).

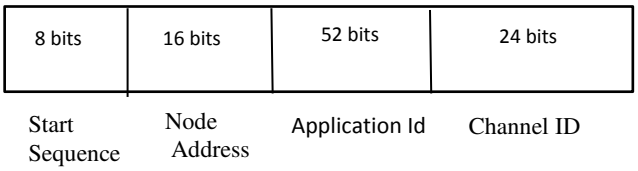

Fig 5: Wake up message format after Manchester encoding

The clock signal is also generated by the circuit. As the packet arrives it first goes to LNA in the front end which amplifies the signal. This signal is then given to detector block. The incoming signal is amplified OOK RF signal. The detector block has to detect the presence and absence of the oscillations. It consists of a rectifying diode and a capacitor. After detector there is a decoder block which decodes the incoming signal for start sequence, node address, application id etc. Once the signal is decoded it goes to digital control block which is the main block in the circuit. A strobe signal activates the LNA block, detector, decoder and bias block. The bias is used for LNA and detector. A signal called as ibs determines whether the circuit should be receiver or base station (transmitter).The Vreg block handles the power supply to all parts. The power on reset hold the circuit in reset until operating conditions are met. The interface block contains control gates for having known values of signals. The data signal is clocked in with clock signal on negative edge of pulse. The control circuit consists of initialization block, decoder, parameter data and clock division block. The block diagram of the circuit is shown in the Fig 6 .

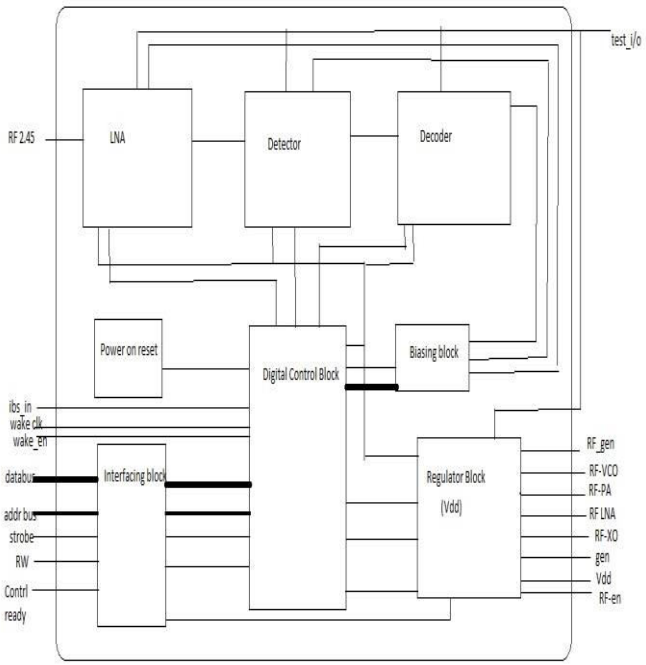

Fig 6: Digital Control Block

When a start sequence is detected, a flag is set and packet reading starts. The node address and the application Id will be checked and if it matches then Verg-en and osc-en is set high. Vreg powers up the controller and RF block. The controller sends ready signal to digital control circuit. If controller ready signal is not set within specific time, osc-en starts oscillator which generates clock signal which acts as watchdog and resets the circuit. After receiving the controller ready signal, the digital control circuit waits for instruction from data bus for read/write, address, and strobe. Then accordingly the circuit will read or write the data (trim parameters) .After completion of data, the controller ready signal becomes low and circuit goes to initial state. Here one cycle is completed. The clock division block handles strobing procedure. It provides strobe signal as per the duty cycle. The implementation is carried out in VHDL. VHDL is Very High Speed Integrated Circuit Hardware Description Language. It is a big and general HDL, and gives various opportunities to describe the same behaviour with different language design. The other HDL is Verilog that is Verify Logic. The source code is written in Xilinx 14.7 version. The test bench is written in Verilog which is used for simulation.[16] The RTL code is synthesized a netlist is created. The netlist is stored as a Verilog/VHDL file and simulated for verification together with a test bench by using the Simulator Verilog-XL /VHDL. The results from the simulations are examined and are reviewed for calculations of power consumption.

3. Experimental Results

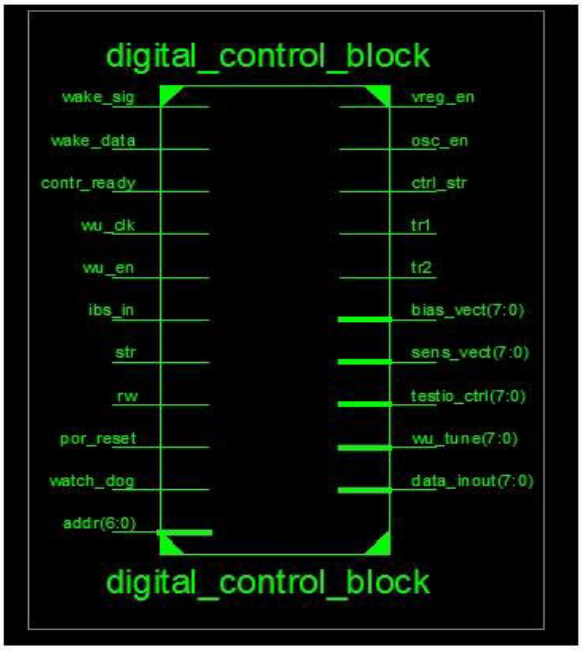

Fig 7: Design of Digital Control Block

In this section the relevant results concerning the complexity of digital control circuit and the performance of the RF transceiver with and without digital control circuit is described. The result focus on architecture of communication controller, output of digital control circuit. The source code is written in VHDL and is synthesized in Xilinx 14.7 software. A package is created for having all constants in the program, predefined at the same place. It is having the advantage that it is easy to change a constant value without any difficulty. The RTL design is shown in Fig 7 below.

The details of the block are shown in fig 8 below.

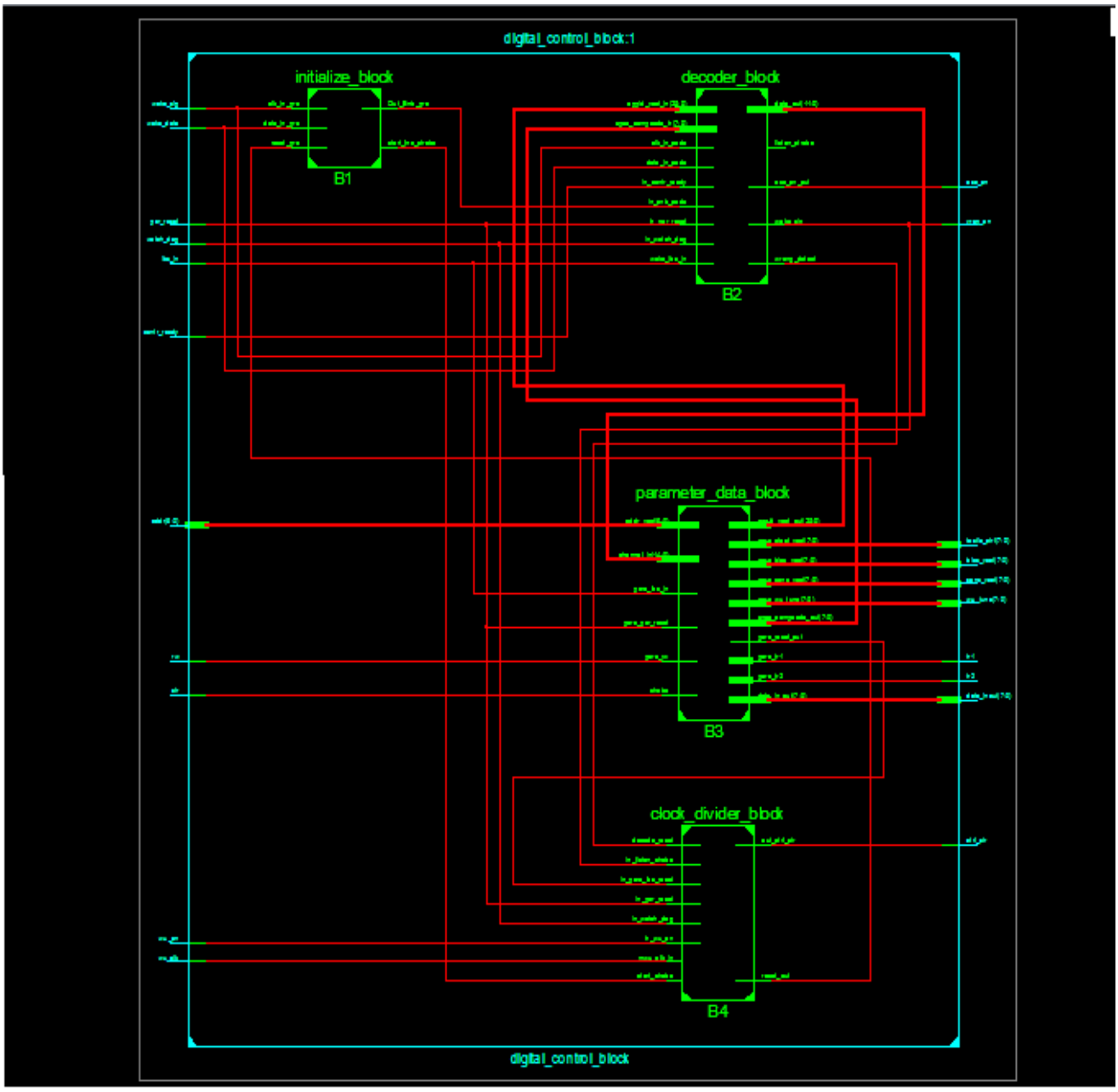

Fig 8: Detailed RTL design of Digital Control Block

Once the RTL design is complete the circuit is simulated with Isim simulator available in the Xilinx software itself. To run the simulation a test bench is written in Verilog-XL. The simulation results are shown in Fig below.

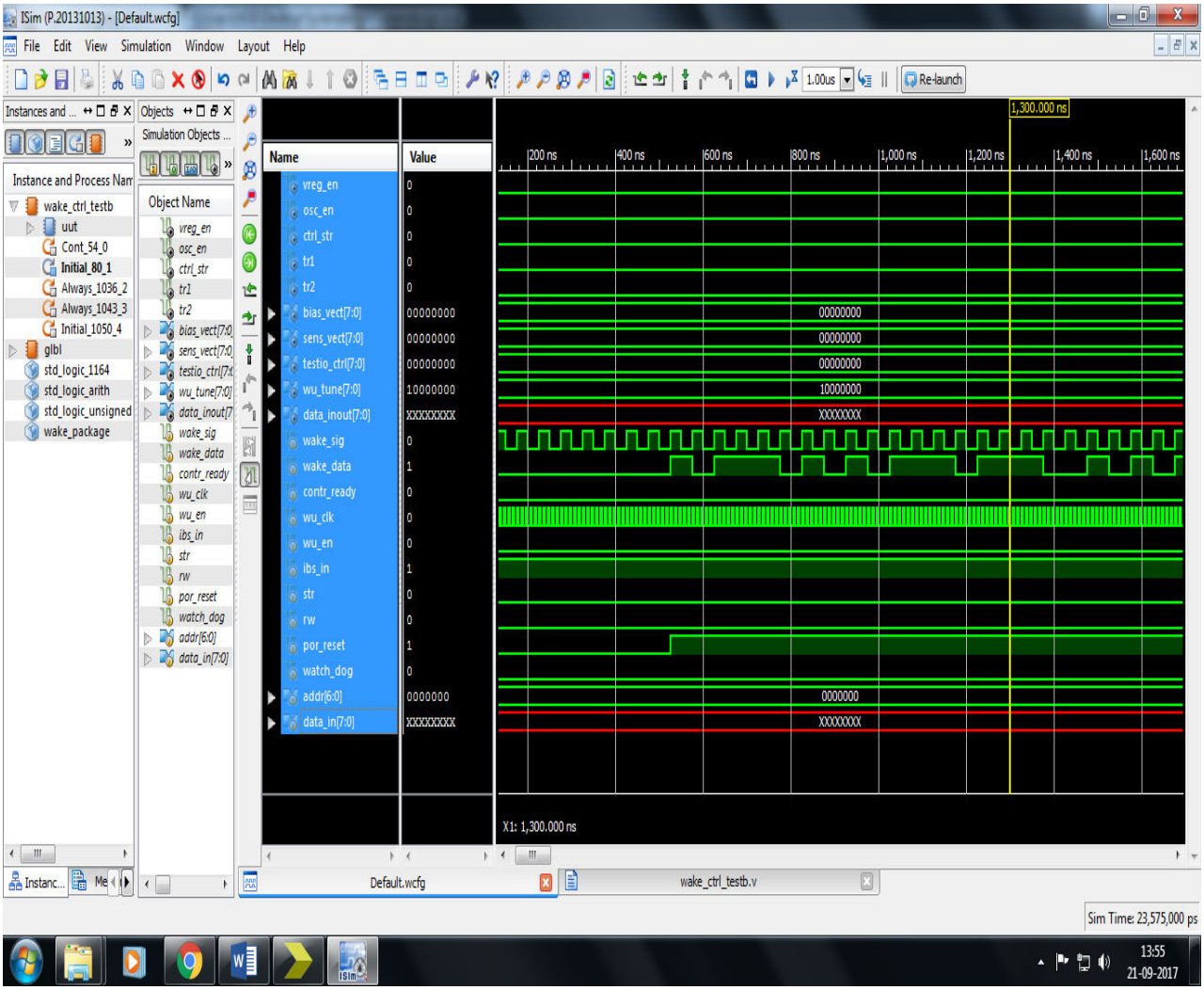

Fig 9 Simulation of Data Signal, Wake Clock, Power on Reset

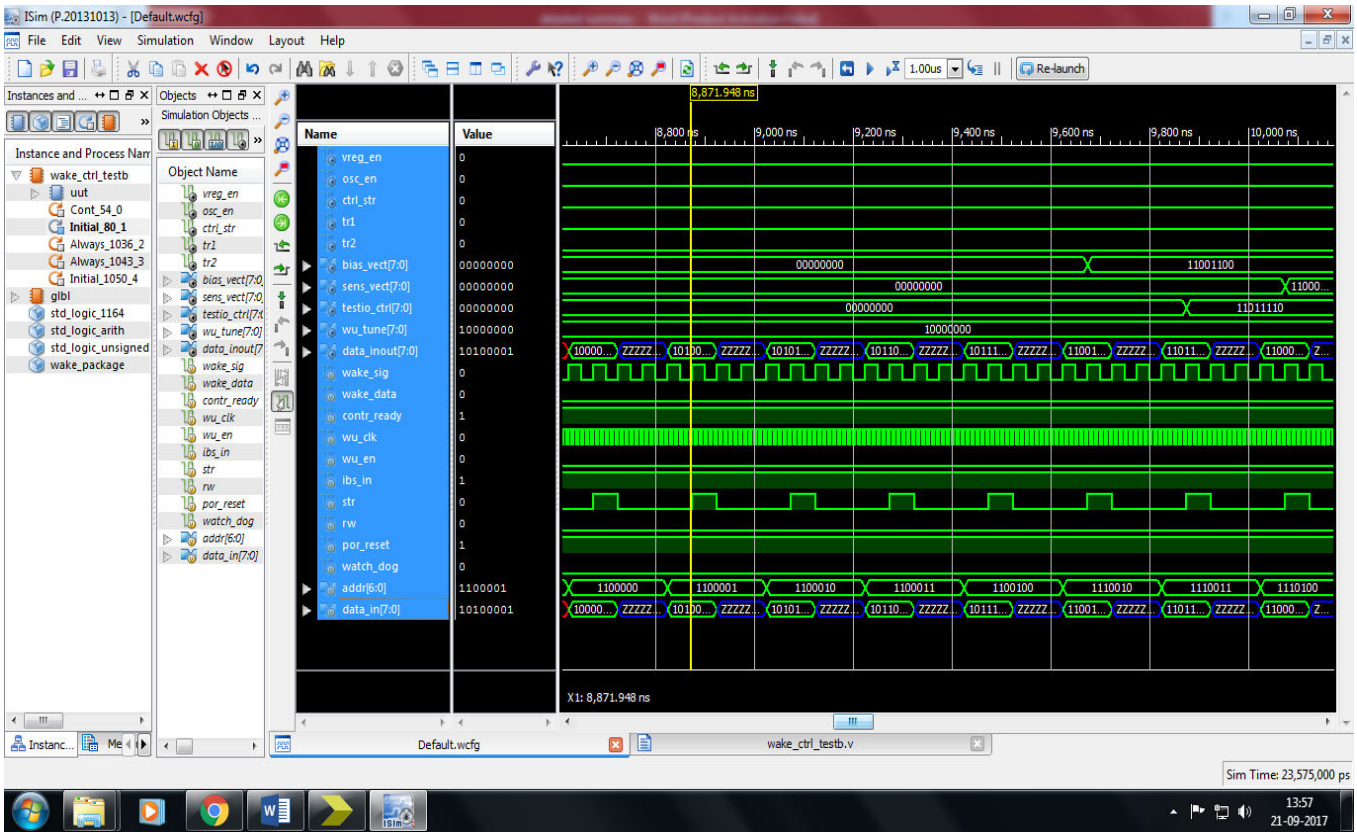

Fig 10 : Writing of trim parameters (rw is 0)

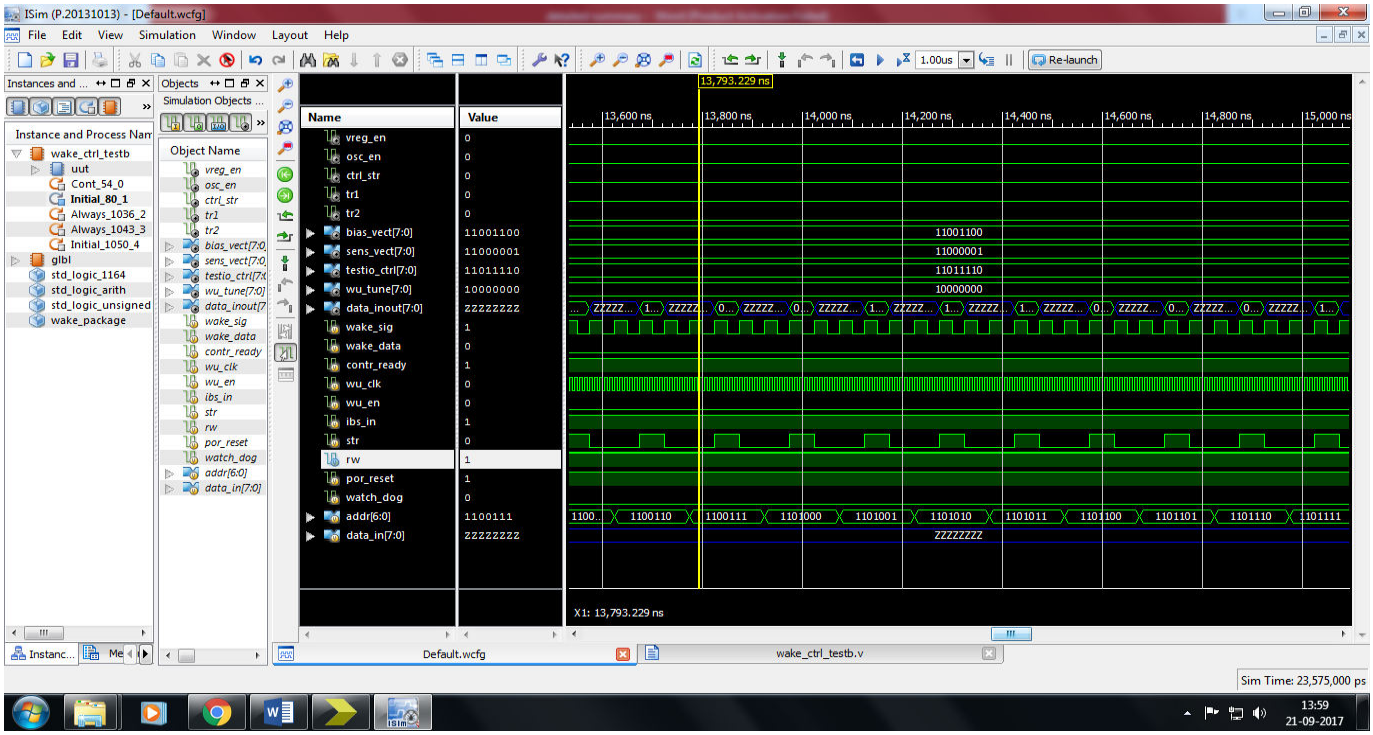

Fig 11 : Reading of trim parameters (rw is 1)

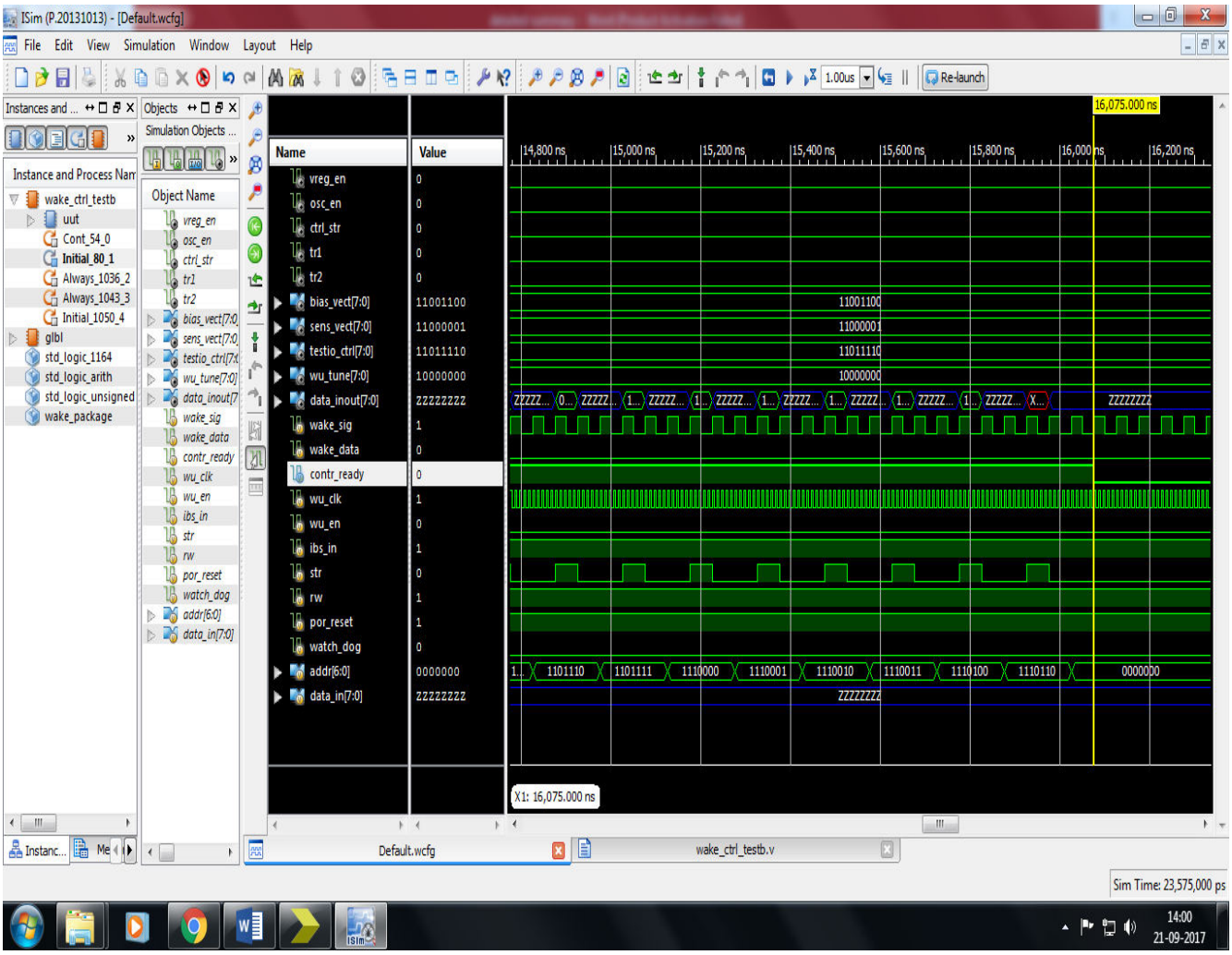

Fig 12: Completion of one cycle (controller ready 0)

The explanation of simulation window can be described as follows

i) The circuit is reset by power on reset.
ii) When the data signal comes the initialization block checks the data pattern.
iii) When the start sequence is detected (at 2.2. microsec) enable signal for decoder block is set high.
iv) The decoder block reads the bits in the packet and decode it to node address, application Id, and channel Id.If node address and application Id matches channel Id is set as output to parameter data block (at 6.6. microsec)
v) At the same time Vreg_en and Osc_en are set high.
vi) When controller ready is set high Osc_en is set low.
vii) The communication with controller on the bus system is started (at 8.3 microsec) as per the instruction either read or write.
viii) Initially writing the data to register starts for all trim parameters and (at 12.6 microsec) reading from the register starts.
ix) The controller ready is set low (at 16.4 microsec) and the whole circuit returns to initial stage. This is completion of one cycle.
x) The total time required from detection of start sequence up to completion of one cycle is 16.4 microsec.

4. Performance Analysis

The performance analysis considering the power consumption is described below. The standard RF transceiver is considered for this analysis. The power consumption for other devices in the sensor node is not considered here. The typical values for CC2500 are given below. (Ref power profile of CC2500 by Ti.Com)

Vcc Range --- 1.8 V to 3.6 V

WOR sleep current ---- 900 nA

Idle current ----- 1.5mA

FSTXon current ----- 7.4 mA

Rx Current ----- 15 mA @ 2.4 kbps

Tx Current ------ 21 mA @ 0db

A) Calculation of power consumption without Digital Control Circuit :
In active mode the power consumption will be sum of Frequency synthesizer calibration, receive and transmit mode and idle state. This can be written as
1.67 uAHr + 31.3 uAHr + 0.04 pAHr
This is equal to
40032.97 x 10^{-6} Ampere hour
Now to calculate Watt Hour. The formula for Watt Hour is
Watt Hour = Ampere-hour x Voltage
The voltage considered here is 1.8 V
So Watt Hour = 40032.97 x10^{-6} x 1.8
Watt Hour = 72059.346 x10^{-6}
Finally Watt = Watthour / hour
Watt = 72059.34 x10^{-6}/3600
Watt = 20.01 x10^{-6} = 20 uWatt

B) Calculation of power consumption with Digital Control Circuit :
In active mode the power consumption will be amount of time required for writing and reading the trim parameters. The total time required to write and read the parameter for digital control circuit is 16.4 micro second as seen from the simulation. The RF transceiver is active for that time only. So power consumption will be
15 mA x 16.4 uA= 246 x10^{-9} /3600 = 0.068 x10^{-9} Ampere Hour
Watt Hour = Ampere-hour x Voltage
The voltage considered here is 1.8 V.
Watt Hour =0.068 x10^{-9} x 1.8 = 0.1224 x10^{-9}.
Watt= Watthour/ hour
Watt = 0.1224 x10^{-9}/ 3600 = 0.034 x 10^{-12} = 0.034pWatt.

The result of performance analysis shows that the power consumed with digital control circuit is less than power consumed without digital control circuit

5. Conclusion

The paper propose the communication centric approach rather than conventional approach for the architecture of WSN. In the development of new RF transceiver a digital control circuit is designed which enables the wake up of main radio only when specific messages is sent. The power consumption of such system should be well below the power consumption of main radio and must wake it up while avoiding false alarm and missed messages. The digital control circuit consists of a front end consisting of LNA, detector and a decoder. The digital control block consists of initialization block, decoder block, parameter data block and clock division block .The wake up message is designed consisting of start sequence (8 bits) .node address(8 bits) , Application Id(26 bits) and Channel Id (12 bits). The Manchester encoding is done on the message so that the message should remain intact or for security purpose .Due to this the packet bits are getting doubled .The start sequence is not encoded. The modulation used OOK modulation so that it is easy to carry out demodulation with the help of passive components at detector stage. The software is written in VHDL and the program is run on Xilinx 14.7. The simulation is carried out in Isim software available with Xilinx. The test bench required for simulation is written in Verilog. The time required to write and read the parameters is calculated from the simulation .The reference RF transceiver used is CC 2500. The specifications for CC2500 are collected from Texas Instruments and the power profile of CC2500 is used for calculation of power consumption. The performance analysis is carried out with and without digital control circuit. The analysis shows that the power consumed without Digital control circuit is approx. 20 uW and the power consumed with digital control circuit is 0.034 pW. The above performance analysis shows that if less power is to be consumed than it is must to keep the microcontroller and RF transceiver in sleep mode unless the correct message arrive at the input . This will be beneficial for the WSN which are remotely placed.

The comparison of previous work done is shown in table below

Table 1: Comparison of previous work done

Ref No	Type of Work	Technology	Carrier Freq	Supply Vol	Power	Year
11	Simulation	FPGA	2.4	0.85 -1.2 (v)	5-30 uW	Springer 2013
12	Realization/ implementation	Mixed ASIC & FPGA	2.4 GHz	1.5 (v)	12.. 5 uW	IEEE 2009
13	Realization/ implementation	ASIC CMOS	2.4 GHz	0.5 (v)	52 uW	IEEE 2009
14	Realization/ implementation	CMOS	2.4 GHz	0.75 (v)	50 uW	IEEE 2014
15	Implementation	CMOS	2.4 GHz	1.8 (v)	3.2 uW	IEEE 2015
Our work	Simulation	FPGA	2.4 GHz	1.8 (v)	0.34 pW	2017

The circuit can have some modification in the future. The wake up massage may have some minor changes .The major structure will remain as it is but changes in sub blocks are possible. Some more digital functions can be added to the circuit .If the parameters are to be changed then it is easy to change them directly in the package. The structure of the code is hierarchical so any block can be added as per the requirement in the program. The work carried out here is up to simulation stage. Next task is to go for layout stage, do the post layout simulation with updated timing files. The hardware implementation can be carried out in near future. The code written in VHDL has to be downloaded on any FPGA kit and the implementation can be done. The

simulation can also be done in Simvision program from Cadence.

References

[1] Feng Zhao, Leonidas Guibas, "Wireless Sensor Networks- An Information processing Approach", Morgam Kaufmann Publishers-An imprint of Elsevier, pp 63-101

[2] Ajay V.Deshmukh "Micro controllers- Theory and Applications" Tata McGraw-Hill Companies, New Delhi, pp 115-202.

[3] E.-Y. Lin, J. Rabaey and A. Wolisz, "Power-efficient rendez-vous schemes for dense wireless sensor networks", in IEEE ICC, Paris, 20–24 June 2004 pp 3769-3776

[4] Raja Jurdak, Member, IEEE, Antonio G. Ruzzelli, and Gregory M.P. O'Hare, "Radio Sleep Mode Optimization in Wireless Sensor Networks," IEEE TRANSACTIONS ON MOBILE COMPUTING, VOL. 9, NO. 7, JULY 2010, pp 955-968

[5] Denis C. Daly, *Student Member, IEEE*, and Anantha P. Chandrakasan, *Fellow, IEEE,"* An Energy-Efficient OOK Transceiver for Wireless Sensor Networks", IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 42, NO. 5, MAY 2007, pp 1003-1011

[6] James Mathews, Matthew Barnes, Alex Young and D. K. Arvind," Low Power Wake-Up in Wireless Sensor Networks using Free Space Optical Communications", Feb 2010 IEEE 2010 Fourth International Conference on Sensor Technologies and Applications,pp 256-261

[7] Qizheng Gu," RF SYSTEM DESIGN OF TRANSCEIVERS FOR WIRELESS COMMUNICATIONS",Springer pp 114-198

[8] Michel C. Jeruchim, Philip Balaban, K. Sam Shanmugan," Simulation of Communication Systems, Modeling, Methodology, and Techniques,Second Edition, KLUWER ACADEMIC PUBLISHERS NEW YORK, BOSTON, DORDRECHT, LONDON, MOSCOW,pp 14-45

[9] Xiongchuan Huang, Pieter Harpe, Guido Dolmans, Harmke de Groot," A 915MHz Ultra-Low Power Wake-Up Receiver with Scalable Performance and Power Consumption,"IEEE 2011, pp 543-546

[10] Nikita patel, Neetu kumari, Satyajit Anand and Partha Pratim Bhattacharya," A Brief Review on Low Power Wake-Up Receiver for WSN", International Journal of Innovative Research in Computer and Communication Engineering, Vol. 1, Issue 9, November 2013,pp2035-2041

[11] Pons Jean-Franc¸ois , Brault Jean-Jules ,Savaria Yvon," Modeling, design and implementation of a low-power FPGA based asynchronous wake-up receiver for wireless applications", Analog Integr Circ.Sig Process (2013) Springer ,pp 169-182,

[12] Macro Spinola Durante, Stefan Mahlknecht," An Ultra low power Wakeup Receiver for Wireless Sensor Nodes", 3rd International Conference on Sensor Technologies and Applications, Sept 2009, IEEE Computer Society ,pp167-170

[13] Nathan M. Pletcher, Simone Gambini, Jan Rabaey," A 52 uW Wake up Receiver with -72 dBm Sensitivity Using an Uncertain –IF Architecture , IEEE Journal of Solid State Circuits Vol 44, No 1,Jan2009,pp 269-280

[14] Carl Bryant, Henrik Sjoland," A 2.45 GHz, 50 uW Wake up Receiver Front end with -88dBm Sensitivity and 250 kbps Data Rate ", IEEE Aug 2014 ,pp235-238

[15] Chandra Shekhar, Shirshu Varma, M. Radhakrishna , "A 2.4GHz Pasive Wake Up Circuit for Power Minimization in Wireless Sensor Nodes", IEEE May 2015,pp 453-458

[16] Robert Bogdan Staszewski and Roman Staszewski Poras T. Balsara, "VHDL Simulation and Modeling of an All-Digital RF Transmitter", Proceedings of the 9th International Database Engineering and Application Symposium (IDEAS'05) IEEE 2005,pp110-116

[17] C. Siva Ram Murthy, B.S.Manoj, "Ad Hoc Wireless Networks Architecture and Protocols", Pearson, pp 585-639

[18] Amit Sharm, Kshitij Shinghal, Neelam Srivastava, Raghuvir Singh, "Energy Management for wireless sensor network odes", International Journal of Advances in Engineering & Technology,Vol. 1, Mar 2011, ISSN: 2231-1963, pp 7-13

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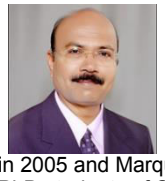

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